Fall 2017 Project Proposal

(Henry Thai Hoa Nguyen)

Big Picture

The goal of my research is to enable design automation in the field of radio frequency (RF) integrated communication circuits and systems. Radio frequency integrated circuit design is a mature field with a lot of research effort spending to optimize performance using sophisticated analog and RF techniques. This research will explore a rather less studied aspect in RFIC design, with emphasis on the design synthesizability rather than transceiver performance. Which means main focus is on a design methodology that allow the transceiver chip to be fully synthesized automatically from some RTL descriptions. And the automation design methodology must also provide a way to correctly estimate and ensure the synthesized transceiver can fulfill a set required performance metrics to enable robust functionality of the radio link. Our approach is by replacing traditional analog/RF circuit blocks and passive elements with only digital and p-cell based implementation as this enables direct synthesis from RTL code with synthesis tools.

As a matter of fact, digital implementation will pose a lot of restriction on circuit and system architecture and hence impact performance metrics of traditional analog/RF blocks. This is a direct trade-off between complexity and performance, which is actually a desirable trade-off that we would like to exploit. Again, the focus here is not on performance optimization but rather on synthesizability and a method to analyze, estimate and ensure the overall required performance for the fully synthesized radio to function properly within the intended wireless protocol. Nevertheless, performance limitation of the synthesizable transceiver still can be further improved in later research stage by employing sophisticated digital correction techniques which are still fully synthesizable.

Another objective as a result of fully synthesizability is that the use of off-chip and passive component as in traditional RFIC design such as crystal oscillator and off-chip antenna will be eliminated. In fact, the research will target low power mm-wave short range radio link so that the normally big size off-chip antenna will become small enough to be implemented on-chip as a standard p-cell. Ultimately, the goal is to come up with a fully synthesizable one-chip integrated radio module compiled entirely from RTL descriptions, based on a standard digital/p-cell library of the available process technology. As a result, the radio design process will only involve the generation of RTL descriptions which is highly abstract and is much more non-technical friendly as the designer no longer has to deal with detail technical aspects of circuit topology, device sizing and layout optimization.

A clear benefit is a significant reduction on the cost in terms of design expertise, design effort and design time. The fully synthesizable one-chip all-digital transceiver will enable any non-expert to quickly generate a complete workable IC radio link within minutes compared to months in a typical transceiver design cycle. This give way to the implementation of ubiquitous wireless network where a radio can be easily integrated with every microcontroller chip to establish a near field, moderate data rate link with another chip. Imagine a wireless evolution where low-bandwidth communication between ICs are no longer through I2C but through these low cost

wireless links. Last but not least, another major advantage of a synthesizable radio is that it can keep up with the fast technology scaling trend since there is virtually no extra effort needed to port a design from one process node to another process node.

Specific project scope

This research will first target on simple low power transceiver architecture in mm-wave (Fig. 1) that will enable wireless link at 2Mbs data-rate of around less than 10cm. Output power at antenna is targeted at 0dBm at 60GHz radio frequency. The proposed single-chip CMOS radio will have no external components, except for a power source, to reduce size, weight, and cost. Perhaps more importantly, this radio will be based on a fully synthesizable design that will allow engineers to add radio functionality to their existing designs with very little additional design effort. To achieve these goals, the proposed radio will employ:

1. all-digital circuit architectures,
2. non-coherent mm-wave communications, and
3. a crystal-less clocking architecture.

While crystal-less clocking eliminates bulky quartz crystals, the use of mm-waves allows small antennae that can be integrated on a CMOS die. The all-digital circuit architectures will allow radio design using blocks from standard digital cell libraries such as inverters, instead of dedicated analog blocks. This may allow a register transfer level (RTL) description of much of the radio that could be readily retargeted to other process technologies. The non-coherent modulation schemes such on/off keying (OOK) significantly simplifies the design of the mm-wave front-ends such that even these analog blocks can be designed with minimal effort. While getting an RTL description for the mm-wave front-end is a long-term goal, this project will approach that by enabling a script-plus-pcell based design for key mm-wave front ends while the rest of the radio would be specified in RTL form.

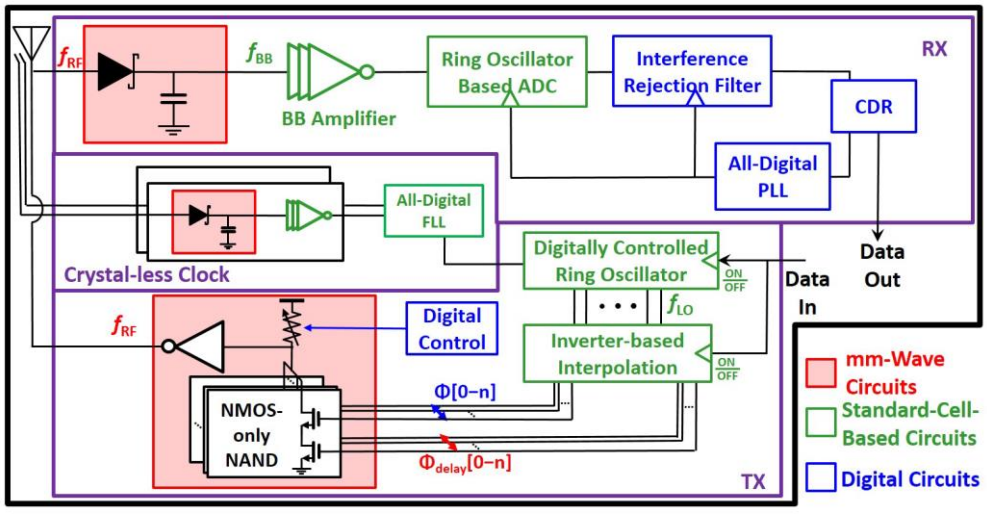

Figure 1: Proposed (almost) synthesizable, single-chip, CMOS mm-wave radio with an on-chip antenna, and crystal-less, antenna-referred clocking. The simple mm-wave blocks will be designed using a script-plus-pcell approach. Other crystal-less references will also be investigated.

For the Fall quarter 2017, our focus will be on the TX RF portion, which includes a 60GHz frequency generator, 60GHz PA and 60GHz integrated on-chip antenna (figure 2). If time allows, we will also look into the implementation of the ring oscillator that generates the multi-phase LO 10GHz clock signals that are the inputs of the 60GHz frequency generator.

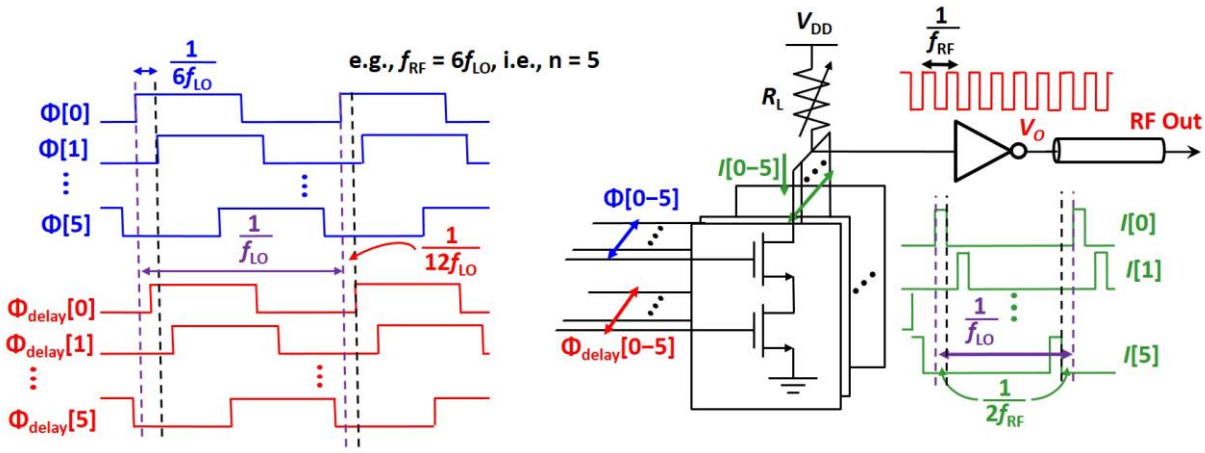

Figure 2: mm-wave TX front-end using multi-phased NMOS-only NAND gates

Background / related work / references

- Regarding synthesizable all-digital transceiver system design:

There are two prominent work on synthesizable all-digital transceiver:

1. R. Y.-K. Su (2011) has demonstrated a synthesized standard-cell radio for indoor applications with spec.:

Table 1.1: Target Specs

Parameter	Specification
Carrier Frequency	ISM (915MHz, 2.4GHz)
Modulation Scheme	FSK/OOK
Data Rate	10kbps
Sensitivity	Better than -70dBm
Active Power Consumption	As low as possible

The transmitter and receiver prototypes are built in a .18μm standard CMOS. The transmitter includes a PA and a fractional-N all-digital PLL with ring oscillator (no crystal required). The PA uses inverter cell and stacked structure design. Target output power is at 0dBm. The fractional-N PLL uses an embedded time-to-digital converter (TDC) with multi-path to increase TDC resolution, and includes digital correction circuitry to resolve issues from clock skew. The TX is also ported to a 65-nm CMOS to verify the synthesizability. The RX front-end uses analog LNA gain of 20 dB. The whole RX SNR and NF is 10 dB. The structure is almost the same as A. Molnar *et al*. (2004)

2. Y. M. Park (2011) showed an ultra-wideband (UWB) transmitter, a time-to-digital converter (TDC), and a PLL in 65nm CMOS technologies as prototypes of cell-based circuits. The UWB transmitters embed the proposed DCO to control the center frequency and width of output pulses in the 3.1GHz-5.0GHz UWB band. The TDC adopts a cyclic Vernier structure, where two DCOs are oscillating with slightly different periods. The TX does not seem to have a PA, instead, it drives an off-chip high-pass filter and is then measured. The core of the thesis is the synthesis methodology and some calibration techniques.

In both of these 2 works, standard-cell approach has been used. However, not all circuit blocks are implemented digitally such as the LNA and PA in second work. This is due to the fairly complicated transceiver architectures that were used. Also, the antenna could not be integrated due to large antenna dimension. Our research will be fundamentally different from these work in 2 major points: First, our research targets simple transceiver architecture which can enable fully digital implementation. Second, our research targets much higher mm-wave frequency range (60GHz) which will lead to much smaller antenna dimension which can then be integrated on-chip and completely eliminate off-chip components.

- Regarding TX RF front-end design: 60GHz pulse generator PA & 60GHz integrated antenna

  The TX front-end will employ a multiplexed transmitter design. As shown in Fig. 2, the TX is made of several NMOS-only NAND gates connected together in wired-OR configuration with a shared load resistance, RL. The gates are driven by distinct phases of a lower frequency LO. For example, to generate 60 GHz output, 12 distinct phases of 10 GHz separated by 100ns/12=8.33ps will drive the transmitter. The generation of the distinct phases of the (10 GHz) LO using digital standard cells is by a ring oscillator which is the most synthesizable means of achieving the multi-phase clock generation. However, the achievable phase separation is limited by the minimum delay of the inverter. The proposed research will employ inverter-based phase interpolation (Madoglio et al. (2012), Ravi et al. (2011), Ravi et al. (2012)), as shown in Fig. 3 to generate phase separation much smaller than the inverter delay. Inverters of different, programmable strengths, driven by adjacent phase signals from the ring oscillator drive a common node. By choosing the relative strength of the inverters, the output phase can be set to be an arbitrary phase value between that of the two inputs.

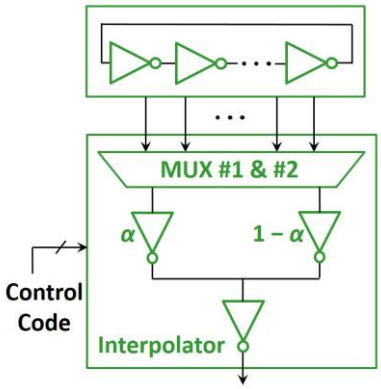

Figure 3: Multi-phase LO generation using inverter-based phase interpolation

Goals, deliverables, tasks

There will be a tape-out with Prof. Pamarti group in UMC 28nm process if they have spare silicon area. So, we can take this opportunity to tape-out a testing prototype of Tx RF front-end to study and verify the feasibility of generating and transmitting a mm-wave 60GHz radio signal in advanced CMOS process. The prototype 60GHz Tx RF design must achieve acceptable performance (Pout) in post layout simulation with all parasitic effects included and also more importantly, the design must be testable by available equipment in the lab when the chip comes back. The scheduled tape-out is on Dec 6th 2017.

Next term plan: If we managed to tape-out a prototype this term, the plan for next term will be focus on the testing, result correlation and debugging/performance improvement…

Below is the detailed weekly planning of this term research plan:

Week	Goals	Deliverables	Tasks
3 (Oct 16th-20th)	+ Gain initial understanding of the Tx RF blocks and process technology. + Understand achievable performance of current available design and any limitation.	+ Initial simulation results to demonstrate operating principle. + Explanations for performance limitations	+ Study current available Tx RF design. + Get hand-on with PDK and design process. + Perform simulations and get performance and the initial design
4 (Oct 23rd-27th)	+ Literature review study + Optimal Tx RF design (using synthesizable circuit)	+ Any Improvement in the performance metrics of Tx RF design. + Perhaps new architecture of pulse generator or output buffer/PA if that leads to better performance	+ Explore different method of 60GHz freq. generation from phase-shifted 10GHz LO signal + Improving output driver PA performance
5 (Oct 30th-Nov 3rd)	+ Optimal Tx RF design (using synthesizable circuit)	+ Any Improvement in the performance metrics of Tx RF design. + Perhaps new architecture of pulse generator or output buffer/PA if that leads to better performance	+ Design and performance optimization (continue)

6 (Nov 6th-10th)	"On-paper" design without parasitic	+ Finalized design of Tx RF. + Finalized achievable performance before parasitic.	+ Finalize the design + Consolidate simulated performance of the chosen Tx RF design (without parasitic) → design review + Start put in parasitic model estimation and on-chip integrated antenna modelling.
7 (Nov 13th-17th)	+Real design with parasitic. +Physical implementation	+ Finalized achievable performance with parasitic. + Layout on-going	+ Start layout + Consolidate simulated performance of the chosen Tx RF design with parasitic effect and antenna model→ design review
8 (Nov 20th-24th)	+ Optimized layout design	+ Finished layout + Final performance with post-layout extracted parasitic	+ Final layout + LVS + DRC verification + Post layout simulation
9 (Nov 27th-Dec1st)	Tape-out ready design	Tape-out ready version of test 60GHz pulse generator + PA + on-chip antenna	+ Post layout simulation (cont.) ➔ Design review
10 (Dec 4th-8th)	Taped-out prototype	Tape out of 60GHz pulse generator + PA + on-chip antenna	+ Tape out

References

1. R. Y.-K. Su, "Towards a synthesizable standard-cell radio," Ph.D. dissertation, Dept. Elec. Eng. Comput. Sci., Univ. California, Berkeley, CA, 2011.
2. A. Molnar *et al*., "An ultra-low power 900 MHz RF transceiver for wireless sensor networks," in *Proc. IEEE CICC*, 2004, pp. 401−404.
3. Y. M. Park, "A cell-based design methodology for synthesizable RF/analog circuits," Ph.D. dissertation, Dept. Elec. Eng. Univ. Michigan, Ann Abor, MI, 2011.
4. Madoglio, P., A. Ravi, H. Xu, K. Chandrashekar, M. Verhelst, S. Pellerano, L. Cuellar, M. Aguirre, M. Sajadieh, O. Degani, H. Lakdawala, and Y. Palaskas (2012), A 20dBm 2.4GHz digital outphasing transmitter for WLAN application in 32nm CMOS, in IEEE International Solid-State Circuits Conference (ISSCC) Digest of Technical Papers, pp. 168–170, doi:10.1109/ISSCC.2012.6176962.